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(72) Inventors:  
• Mastromatteo, Ubaldo  
20010 Bareggio (IT)  
• Ferrari, Paolo  
21013 Gallarate (IT)

(71) Applicant: STMicroelectronics S.r.l.  
20041 Agrate Brianza MI (IT)

(74) Representative: Cerbaro, Elena et al  
c/o Studio Torta S.r.l. Via Viotti, 9  
10121 Torino (IT)

(54) Process for manufacturing a through insulated interconnection in a body of semiconductor material

(57) The process for manufacturing a through insulated interconnection is performed by forming, in a body (1) of semiconductor material, a trench (2) extending from the front (7) of the body (1) for a thickness portion thereof; filling the trench with dielectric material (6); thinning the body starting from the rear (5) until the trench (2), so as to form an insulated region (3) surrounded by

dielectric material; and forming a conductive region (8, 25, 28, 30b) extending inside said insulated region (3) between the front and the rear of the body and having a higher conductivity than the first body (1). The conductive region (8, 25, 28, 30b) includes a metal region (25, 28) extending in an opening (24) formed inside the insulated region (3) or of a heavily doped semiconductor region (30b), made prior to filling of the trench.

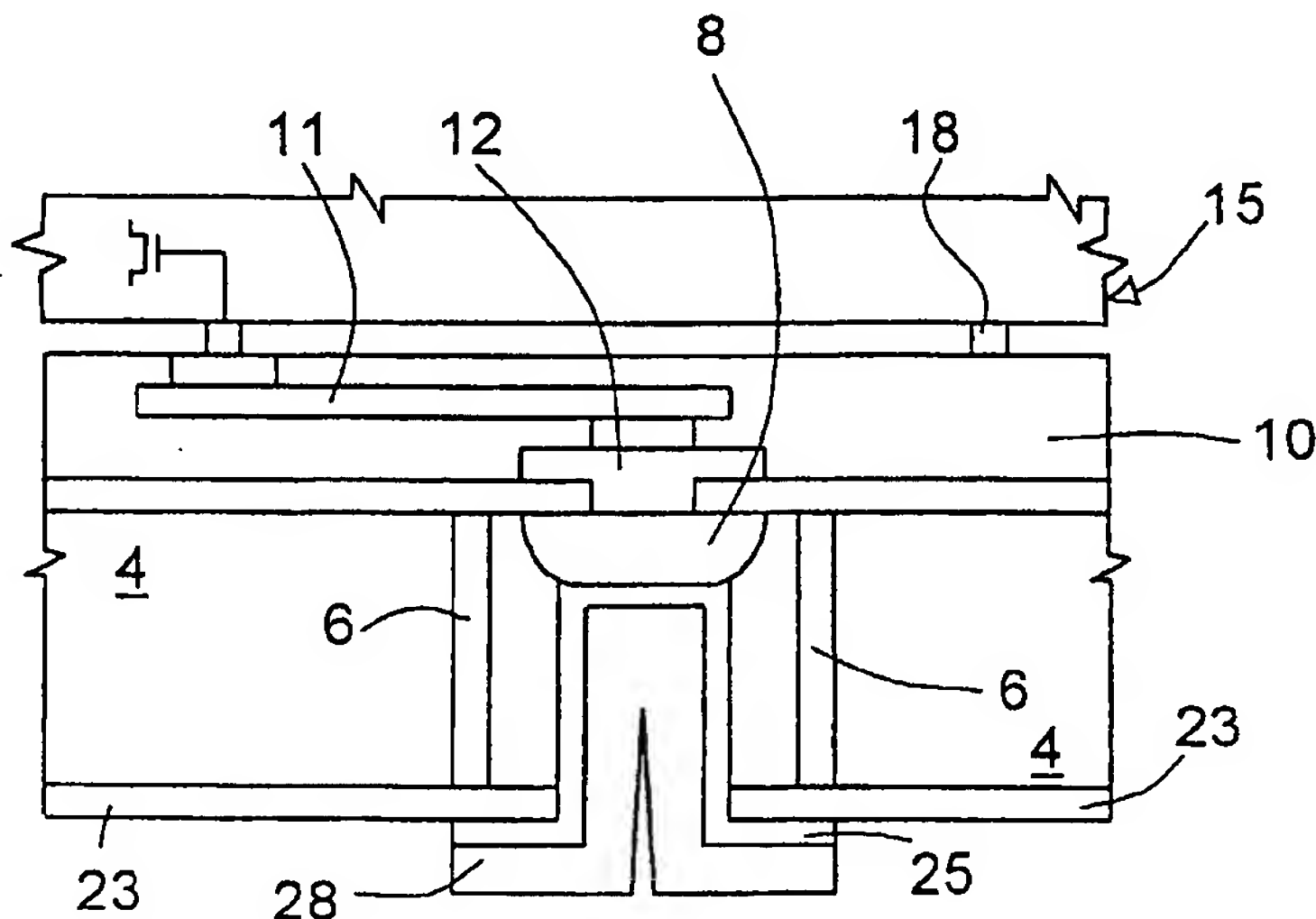


Fig. 8

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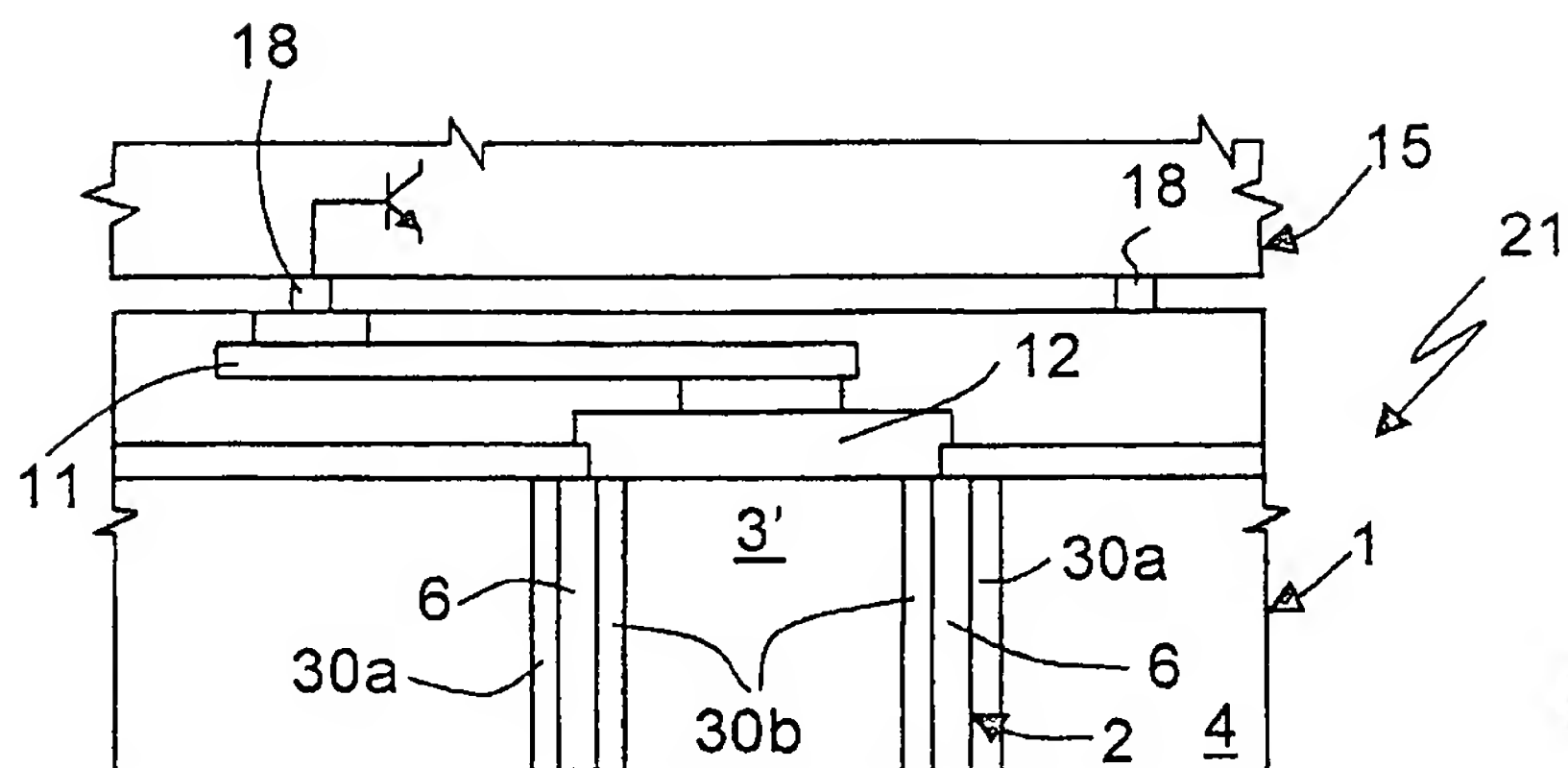


Fig. 12

## Description

[0001] The present invention relates to a process for manufacturing a through insulated interconnection in a body of semiconductor material.

[0002] As is known, for manufacturing microsystems comprising elements obtained using different technologies, such as Microelectromechanical systems (MEMS) and integrated circuits, there exists the need to electrically connect two opposite faces (front and rear) of substrates integrating electronic components or, generally, carrying passive elements and/or protection structures and/or connection structures to other substrates.

[0003] EP-A-0 926 723 describes a process for forming front-rear through contacts in micro-integrated electronic devices. According to this process, a metal contact region extends through a through opening in the chip. In detail, this process is basically made up of the following steps:

1. Formation of metal connection regions on the front of a wafer during formation of the contacts of the device; the metal connection regions are formed at the location where the connection with the rear of the wafer will be made;

2. Etching of the rear of the wafer for partial removal of the substrate in the connection locations with formation of openings passing right through the wafer;

3. Deposition of an insulating layer on the bottom and on the walls of the through cavities;

4. Removal of the insulating layer from the bottom of the cavity to obtain contact areas with the front of the wafer and with the metal connection regions;

5. Deposition or growth from the rear of a metal layer, which coats the walls of the cavities, makes electrical contact with the metal connection regions, and has surface portions on the rear of the wafer;

6. Formation on the rear of connection regions towards the outside in electrical contact with the surface portions.

[0004] In the process described above, the biggest difficulties lie in insulating the through openings (deposition of oxides, nitrides or polymeric materials), in that they have a depth of several tens of microns and have substantially vertical walls.

[0005] EP-A-1 151 962 describes a structure for electrical connection between two bodies of semiconductor material obtained by digging trenches of a closed (annular) shape from the front of a first, heavily doped, wafer and filling the trenches with dielectric material. Next, the first wafer is thinned from the rear until the trenches are reached, so obtaining an insulated-silicon area (sil-

icon plug), which connects the front and the rear of the wafer. Next, the first wafer is fixed to a second wafer housing integrated components. If MEMS are made in the first wafer, it can be used as protection for the MEMS and their connection to the second wafer.

[0006] In the above structure, the need to dope the first wafer heavily to reduce resistance of the silicon plugs limits the applicability of this solution. In particular, in the first wafer, only some types of microsystems may be integrated, and normally the integration of active components is not possible.

[0007] The aim of the present invention is therefore to provide a process that will enable a front-rear connection of a wafer of semiconductor material in a simple way and without limiting the type of structures that can be integrated in the wafer.

[0008] According to the present invention, there is thus provided a process for manufacturing a through insulated interconnection, as well as an integrated electronic device, as defined in Claim 1 and Claim 18, respectively.

[0009] For a better understanding of the present invention, a number of preferred embodiments will now be described, purely by way of non-limiting example, with reference to the attached drawings, in which:

- Figure 1 is a perspective cross-section of a wafer of semiconductor material during an initial fabrication step;
- Figures 2 to 5 are cross-sections of the wafer of Figure 1, in subsequent fabrication steps;
- Figures 6 to 8 are cross-sections, at an enlarged scale, of a portion of the wafer of Figure 4, in subsequent fabrication steps;
- Figure 9 is a cross-section of a composite wafer according to a variant of Figure 8;
- Figure 10 is a perspective cross-section of a wafer of semiconductor material, in an initial fabrication step, according to a different embodiment of the invention;
- Figures 11 and 12 are cross-sections of the wafer of Figure 10, in subsequent fabrication steps;
- Figure 13 is a cross-section of a composite wafer integrating a fingerprint sensor, obtained using the technique illustrated in Figures 10 to 12; and
- Figure 14 illustrates a variant of Figure 9.

[0010] With reference to Figure 1, a first wafer 1 comprising a substrate 4 of semiconductor material, typically monocrystalline silicon doped in a standard way, for example a P-type <100> substrate with a resistivity of 15  $\Omega/\text{cm}$ , having a first surface 7 and a second surface 5, has undergone steps for making trenches, according to what is described in the above-mentioned patent application EP-A-1 151 962. In particular, the first wafer 1 has been masked and etched to form deep trenches 2 having a closed shape and surrounding cylindrical regions 3 of monocrystalline silicon. The trenches 2 may

have a depth of, for example, 50-100  $\mu\text{m}$ .

[0011] Next (see Figure 2), the trenches 2 are filled, either completely or partially, with insulating material 6, for example, silicon dioxide. For this purpose, a silicon dioxide layer is deposited or grown, and is then removed from the first surface 7 of the first wafer 1 to obtain the structure of Figure 2.

[0012] In a known way (see Figure 3), using implantation, diffusion, deposition and growth steps, inside and on the first surface 7 of the substrate 4 conductive and/or insulating regions are formed, such as to obtain electronic components 9 (schematically represented in Figure 3) according to the circuit that is to be obtained.

[0013] In addition, the surface area of the cylindrical regions 3 is doped, so as to reduce the resistivity, thus forming contact regions 8. The contact regions 8 are preferably made simultaneously with diffused areas in the substrate 4.

[0014] Next, on top of the first surface 7, insulating layers 10 and metal connection regions 11 are deposited. In the illustrated example, a connection region 11 electrically connects, via contacts 12, 13, the contact region 8 to a top surface 14 of the wafer.

[0015] Next (see Figure 4), the first wafer 1 is bonded to a second wafer 15 comprising at least one substrate 16. The substrate 16 houses conductive and/or insulating regions, which form electronic components 20 (also represented schematically). The substrate 16 may be coated with an insulation and/or passivation layer (not illustrated) housing metal contact regions.

[0016] The bonding technique may be direct, by means of palladium/silicon bonds; alternatively, as illustrated in Figure 4, bonding regions 18 are provided of a suitable material, for example, gold, to form a gold/silicon eutectic, as described in the above-mentioned patent application EP-A-1 151 962, or else a low-melting alloy may be used, such as gold/tin. In this way, the composite wafer 21 is obtained formed by the first wafer 1 and the second wafer 15.

[0017] Next (see Figure 5), the first wafer 1 is thinned from the rear mechanically, for example, by grinding, until the bottom of the trenches 2 are reached, preferably until a thickness of less than 100  $\mu\text{m}$  is obtained, for example 50  $\mu\text{m}$  up to 30  $\mu\text{m}$ . The first wafer 1 thus has a second surface 22 opposite to the first surface 7 of the substrate 4, and the cylindrical regions 3 are now insulated from the rest of the substrate 4.

[0018] The second surface 22 is then coated with a dielectric layer 23, which is preferably deposited, for insulation of the rear (see Figure 6).

[0019] Using a mask (not shown), the substrate 4 of the first wafer is dug to form openings 24 extending inside the cylindrical regions 3, as illustrated in the enlarged detail of Figure 6. Preferably, the openings 24 reach the contact regions 8. If these latter regions are not present, the openings 24 may extend until they touch the first surface 7 of the substrate 4.

[0020] Next (see Figure 7), a seed layer 25 is depos-

ited on the rear of the first wafer 1, with the aim of favoring the subsequent galvanic growth of metal contact regions. For instance, the seed layer 25 can be obtained by dipping the composite wafer 21 in a bath of palladium, so as to get the palladium to precipitate on top of the dielectric layer 23 and on the walls and on the bottom of the openings 24, and then by depositing gold by reduction (Wet Pd + Au electroless process), or else by low-pressure chemical vapor deposition (LPCVD) of tungsten, or else by phase vapor deposition (PVD) of titanium (Ti sputtering technique).

[0021] Next, a dry resist layer (not illustrated) is deposited and shaped, to delimit the areas of the rear of the composite wafer 21 where the galvanic growth is to be obtained, and through contact regions 28 are galvanically grown. For instance, the through contact regions 28 may be made of copper or gilded nickel (Ni/Au). In particular (see Figure 8), the through contact regions 28 grow inside the openings 24, which can be filled completely or not.

[0022] Next, the dry resist layer is removed, and the seed layer 25 is removed, where it is not covered by the through contact regions 28. In this way, the structure illustrated in Figure 8 is obtained, which shows a through contact region 28 that enables connection of the rear of the first wafer 1 to the front of the same first wafer and with the second wafer 15, through a contact region 8, a metal connection region 11 and contacts 12, 13.

[0023] The process may continue with the formation of bumps on the rear in direct electrical contact with the through contact regions 28. The bumps, for example of gold/tin, may be deposited in a known way using special (electroplating) machines.

[0024] The formation of a through-contact structure comprising an insulating region obtained by filling a trench with dielectric material and a metal conductive region inside the insulating region guarantees an excellent insulation (greater than 1000 V) of the conductive region with respect to the rest of the substrate, as well as high reliability.

[0025] Should it be necessary to have a greater resistance to high voltages or should there be necessary a capacitive decoupling between the through conductive region and the rest of the substrate, it is possible to provide multiple insulation structures, as illustrated in Figure 9, wherein a second trench 2a, also filled with dielectric material 6a, is present outside the trench 2 and concentrically thereto. The structure of Figure 9 may be obtained adopting the same procedure described above, with the only caution of providing two concentric trenches 2 and 2a simultaneously and filling both of them with dielectric material.

[0026] The illustrated structure presents extremely low resistance thanks to the use of metal and to the shortness of the connection between the front and the rear of the first wafer 1.

[0027] The present invention allows working the wafer from the rear, for example to form integrated compo-

nents, in which the second wafer 15 (which has a normal thickness of, for example, 675  $\mu\text{m}$  for a diameter of 150 mm) may in turn contain integrated components or just have a function of mechanical support during handling of the first wafer.

[0028] The operations on the rear may all be carried out at low temperature (except, possibly, for the deposition of dielectric material using the plasma-enhanced chemical vapor deposition (PECVD) technique), and consequently do not interfere with any components that may have been made on the front of the first wafer 1 or in the second wafer 15.

[0029] The presence of the contact region 8 enables complete digging of the first wafer 1 to be avoided, and hence simplifies the digging operations and reduces the brittleness of the first wafer 1 itself.

[0030] Should it be necessary to have a through-contact structure with very low resistivity, such as the one described previously, it is possible to provide, inside the insulating region 3, doped silicon connections, according to the embodiment described hereinafter.

[0031] In detail, initially, the first wafer 1 undergoes a trench etch, in a way similar to the above. Also in this case, the first wafer 1 comprises a standard substrate 4, of any thickness and any resistivity, so as to be able to integrate standard electronic components. Consequently, at the end of the etching process, the first wafer 1 has trenches 2 surrounding cylindrical regions 3, as illustrated in Figure 1.

[0032] Next, as shown in Figure 10, maintaining the masking layer used for the trench etch, the wafer is doped in an oven. Given the protection of the first surface 7 of the substrate 4 through a protective layer 16 (for example, a silicon dioxide layer), the dopant species diffuse only inside the trenches 2, as indicated by the arrows in Figure 10. Consequently, on the outer walls and on the inner walls of the trenches 2, outer annular portions 30a and inner annular portions 30b are formed connected, underneath the trenches 2, by bottom portions 30c. The cylindrical regions 3 now comprise each a central region 3', doped in a standard way, and an inner annular portion 30b.

[0033] Next (see Figure 11), the trenches 2 are filled with insulating material 6, in a manner similar to the above, and the structure is planarized.

[0034] Then the electronic components, the insulation layers 10 on the front of the wafer, the contacts 12, 13, and the metallizations 11 are made, and the first wafer 1 is bonded to the second wafer 15. Here, each contact 12 is an electrical contact with at least the respective inner portion 30b (in this case it may have an annular shape) or with the entire area of the cylindrical region 3 (including both the inner portion 30b and the central region 3').

[0035] Next (see Figure 12), the first wafer 1 is thinned from the rear, until at least the trenches 2 are reached. In this way, the bottom portions 30c are removed, and the outer portion 30a and inner portion 30b are no longer

electrically connected together. In practice, each central region 3' is now surrounded by a conductive region or via 30b, formed by a respective inner annular portion 30b and insulated from the rest of the first wafer 1 by the insulating material 6.

[0036] Next, the first wafer undergoes further fabrication steps, which include the possible formation of components on the rear, and the formation of contacts and/or bumps on the rear.

[0037] According to the above solution, by making trenches having an internal diameter of 10  $\mu\text{m}$ , with a final thickness of the first wafer 1, after thinning-out, of 100  $\mu\text{m}$ , the vias 30b have a resistance R of:

$$R = R_{\square} \frac{100}{2\pi \cdot 10} = 1,6 R_{\square}$$

where  $R_{\square}$  is the layer resistance of the conductive regions 30b, obtained thanks to doping. For instance, by doping the substrate 4 with  $\text{POCl}_3$ , it is possible to obtain layer resistances of less than 1  $\Omega/\square$ , and hence resistances R in the region of 1 to 2  $\Omega$ . By increasing the radius of the cylindrical regions 3 to a few tens of microns and by reducing the thickness of the first wafer 1 after thinning, to 50  $\mu\text{m}$ , vias 30b with a resistance of down to 100 m $\Omega$  are obtained.

[0038] The embodiment illustrated in Figures 10 and 11 may be used for forming a sensor for fingerprints directly on the rear of the wafer, which houses the control circuitry and processing of the signals, as shown in Figure 13.

[0039] The device illustrated in Figure 13 comprises a first wafer 1, which integrates the components and the electrodes necessary for operation of the sensor, and a second wafer 15, which has purely a supporting function, in order to enable handling of the first wafer 1. On the rear of the first wafer 1, the electrodes are formed. In particular, the reference number 40 designates sensing electrodes for capacitive detection of fingerprints, and the reference number 42 designates electrodes for biasing of the skin. The sensing electrodes 40 are insulated from the environment by a passivation layer 41, while the biasing electrodes 42 are not covered, so as to enable application of the necessary biasing voltages to the skin. The sensing electrodes 40 and the biasing electrodes 42 are connected to the front of the first wafer 1 through the vias 30b, which are made in the way described with reference to Figures 10 to 12. The contacts 44 formed on the front connect the vias 30b to the integrated components designated as a whole by 43. The integrated components 43 are made on the front of the first wafer 1 and comprise diffused regions 45.

[0040] The front of the first wafer 1 is covered by an insulation and protection region 46, on top of which there is formed an adhesive region 47 and contact pads 48.

[0041] The second wafer 15 is bonded to the first wafer 1 at the adhesive region 47, and has cavities 50 facing the first wafer 1 at the contact pads 48. The cavities

50 are formed prior to bonding of the wafers 1, 15 on the front of the second wafer 15.

[0042] Figure 13 also shows scribing lines 55, along which, using a diamond blade, the wafer is cut to obtain a plurality of sensors. The portions of the second wafer 15 on top of the cavities 50 are further removed at the lines 56, for example, by reactive ion etching (RIE) to form a trench etch, so as to enable access to the contact pads 48.

[0043] In practice, the through contact structure according to Figures 10 to 13 comprises, in a way similar to the solution illustrated in Figures 1 to 9, an insulating region 6, obtained by filling a trench with dielectric material, and a conductive region 30b, formed inside the insulating region. In this case, unlike the first solution, the conductive region is formed by a via made of heavily doped semiconductor material. Also in this case, an excellent insulation of the via from the rest of the substrate, as well as high reliability, is obtained, and in the case where an even higher breakdown voltage is required, it is possible to make a double insulation of the type illustrated in Figure 9. For this purpose, using an additional mask, two mutually concentric trenches 2, 2a are made, and doping is performed in the oven only of the more internal trench (Figure 14).

[0044] Finally, numerous modifications and variations may be made to the process and device described and illustrated herein, all falling within the scope of the invention, as defined in the attached claims. For instance, it is possible to repeat the described steps, bonding the composite wafer 21 to a third wafer, in which the trenches have already been formed and filled and in which the electronic components and the corresponding connections have already been made, then thinning the third wafer and making the through conductive regions before or after bonding and thinning. By repeating the above operations even a number of times, it is possible to make a stack of wafers piled on top of one another and connected together by conductive regions that are insulated from the rest of the respective wafer and have a much lower conductivity than that of the respective wafer.

#### Claims

1. A process for fabrication of a through insulated interconnection, comprising the steps of:

- in a first body (1) of semiconductor material having a thickness, a first and a second surface (7, 5), forming a first trench (2) extending from said first surface (7) of said first body (1) for a portion of said thickness;
- filling said first trench with dielectric material (6); and
- thinning said first body starting from said second surface (5) until said first trench (2), so as

to form a thinned body, having a third surface (22) and housing an insulated region (3) surrounded by said dielectric material;

characterized by the step of forming a conductive region (8, 25, 28, 30b) extending inside said insulated region (3) between said first surface (7) and said third surface (22) and having conductivity higher than said body (1).

2. The process according to Claim 1, wherein said step of forming a first trench (2) comprises etching said body (1) along a closed line.
3. The process according to Claim 1 or Claim 2, wherein said body (1) has a resistivity of between 1  $\Omega/\text{cm}$  and 100  $\Omega/\text{cm}$ .
4. The process according to any one of Claims 1 to 3, comprising, prior to said step of thinning, the step of forming, in said body (1), integrated electronic components (9) facing one another and/or on top of said first surface (7).
5. The process according to any one of Claims 1 to 4, further comprising the step of forming at least one further trench (2a) surrounding said first trench (2) and filling said further trench (2a) with insulating material (6).
6. The process according to Claim 5, wherein said steps of forming a first trench (2) and a further trench (2a) are performed simultaneously and said steps of filling said first trench (2) and said further trench (2a) are performed simultaneously.
7. The process according to any one of Claims 1 to 6, further comprising the step of bonding a supporting body (15) on said first surface (7) of said first body (1) prior to said step of thinning.
8. The process according to Claim 7, further comprising the steps, prior to said bonding step, of forming integrated electronic components in said supporting body (15) and forming interconnection and bonding regions (18) on top of said first surface (7) and/or on top of a surface of said supporting body (15) facing said first surface.
9. The process according to any one of Claims 1 to 8, wherein said step of forming a conductive region (8, 25, 28; 30b) comprises forming a contact region (25, 28) of metal material.
10. The process according to Claim 9, wherein said step of forming a contact region (25, 28) comprises forming an opening (24) in said insulated region (3), starting from said third surface (22) up to the prox-

imity of said first surface (7), and forming said contact region inside said opening.

11. The process according to Claim 10, wherein said step of forming a contact region (25, 28) comprises forming a seed layer (25) covering said third surface (22) and side walls and a bottom wall of said opening (24); and selectively growing a metal layer (28) on top of said seed layer.

12. The process according to Claim 10 or 11, wherein, before said step of thinning, the step is performed of doping (8) a surface portion of said first body (1) inside said insulated region (3), and wherein said step of forming an opening (24) comprises digging said thinned body (1), starting from said third surface (22) until said surface portion (8) is reached.

13. The process according to Claim 12, wherein said step of doping is performed simultaneously with a step of forming electronic components (9) in said first body (1).

14. The process according to any one of Claims 1 to 8, wherein said step of forming a conductive region (8, 25, 28; 30b) comprises forming a contact region (30b) of semiconductor material having a higher doping level than said first body (1).

15. The process according to Claim 14, wherein said step of forming a contact region (30b) is performed prior to said step of thinning said first body (1).

16. The process according to Claim 14, wherein said step of forming a contact region (30b) is performed prior to said step of filling (6) and comprises doping said first body (1) in the proximity of side walls of said first trench (2) to form a via (30b) of semiconductor material contiguous to said trench.

17. The process according to Claim 16, wherein said step of doping is carried out in an oven.

18. An integrated electronic device, comprising:

- a first body (1) of semiconductor material having a first face (7) and a second face (5);
- a first trench (2) extending through said first body between said first and said second faces; and
- a dielectric material (6) filling said first trench (2), said dielectric material electrically insulating an insulated region (3) from the rest of said first body (1);

characterized by a conductive region (8, 25, 28; 30b) having a higher conductivity than said first body and extending inside said insulated region (3)

between said first face (7) and said second face (5).

19. The device according to Claim 18, wherein said first body (1) has a resistivity of between 1  $\Omega/\text{cm}$  and 100  $\Omega/\text{cm}$ .

20. The device according to Claim 12, further comprising at least one further trench (2a) surrounding said first trench (2) and filled with insulating material (6).

21. The device according to any one of Claims 18 to 20, comprising a second body (15) bonded to said first face (7) of said first body (1).

22. The device according to any one of Claims 18 to 21, wherein said first body (1) houses integrated electronic components (9) facing one another and/or extending above said first face (7).

23. The device according to any one of Claims 18 to 22, wherein said conductive region (8, 25, 28; 30b) comprises a contact region (25, 28) of metal material.

24. The device according to Claim 22, further comprising a semiconductor region (8) extending inside said insulated region (3) and facing said first face (7), said semiconductor region having a higher doping level than said first body (1) and being in direct electrical contact with said contact region (25, 28) of metal material and with electrical-connection regions (11-13) formed on top of first face.

25. The device according to any one of Claims 18 to 22, wherein said conductive region (8, 25, 28; 30b) comprises a contact region (30b) of semiconductor material having a higher doping level than said first body (1).

26. The device according to Claim 25, wherein said conductive region comprises a via (30b) contiguous to said insulating material (6).

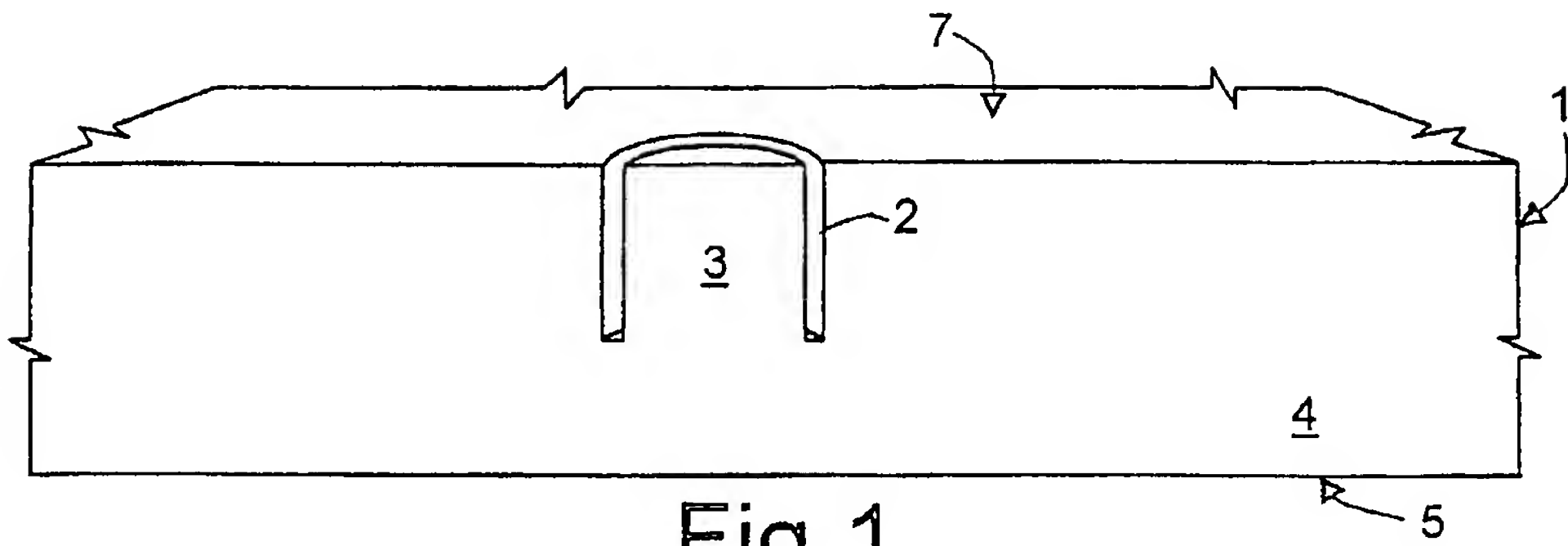


Fig. 1

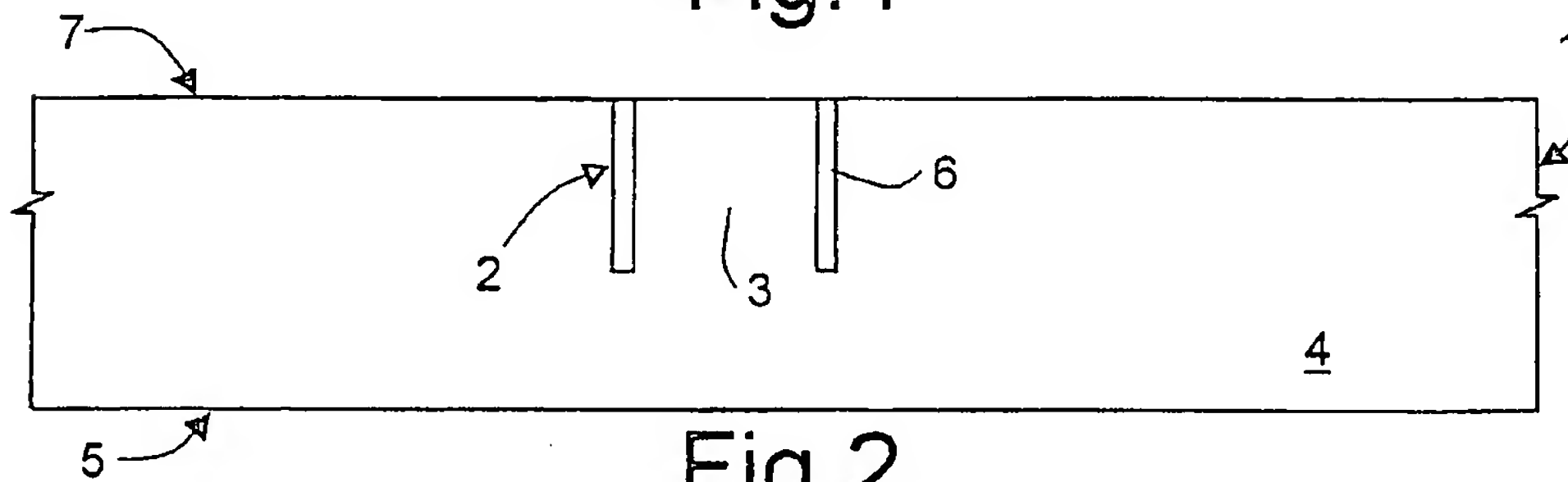


Fig.2

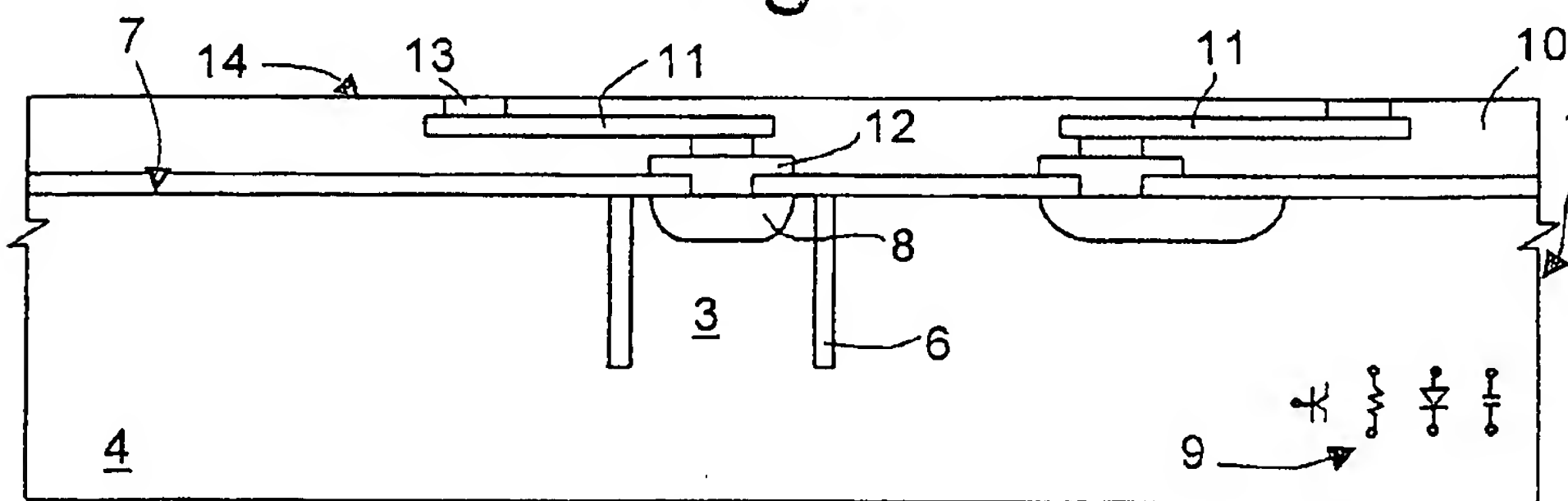


Fig.3

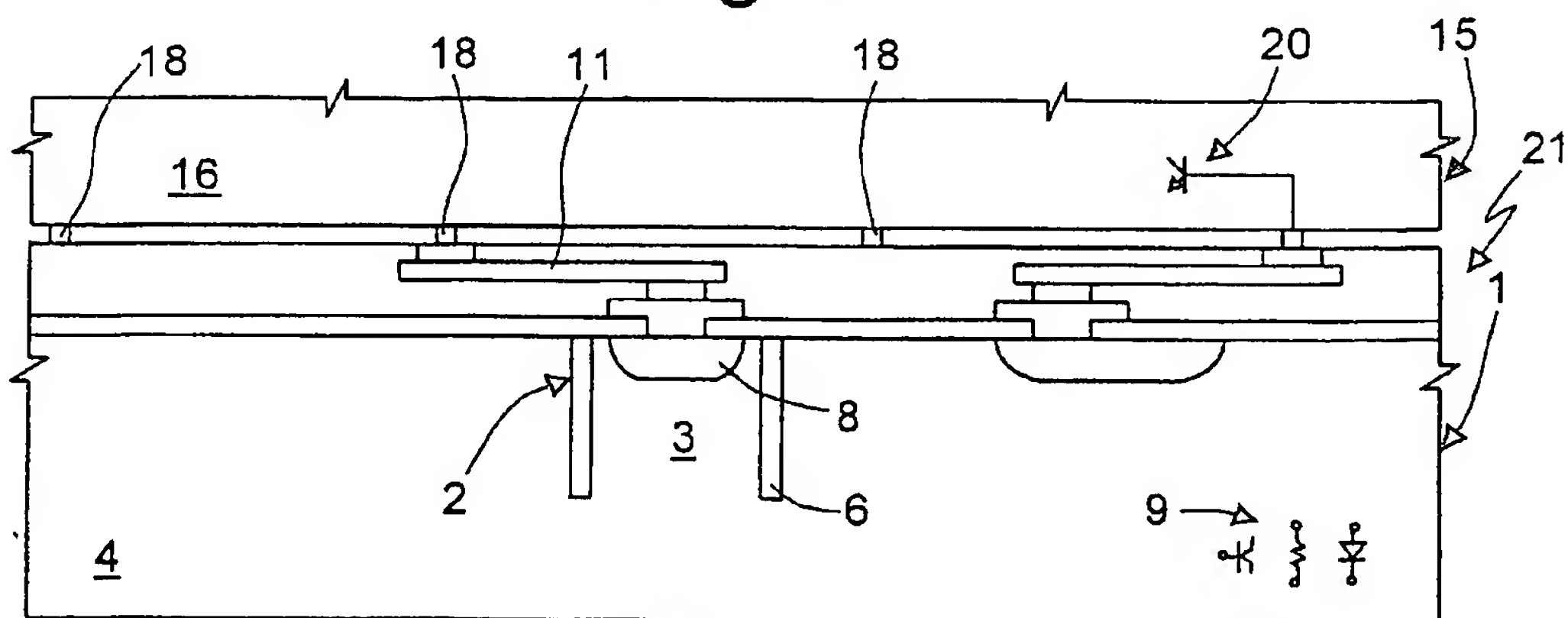


Fig.4

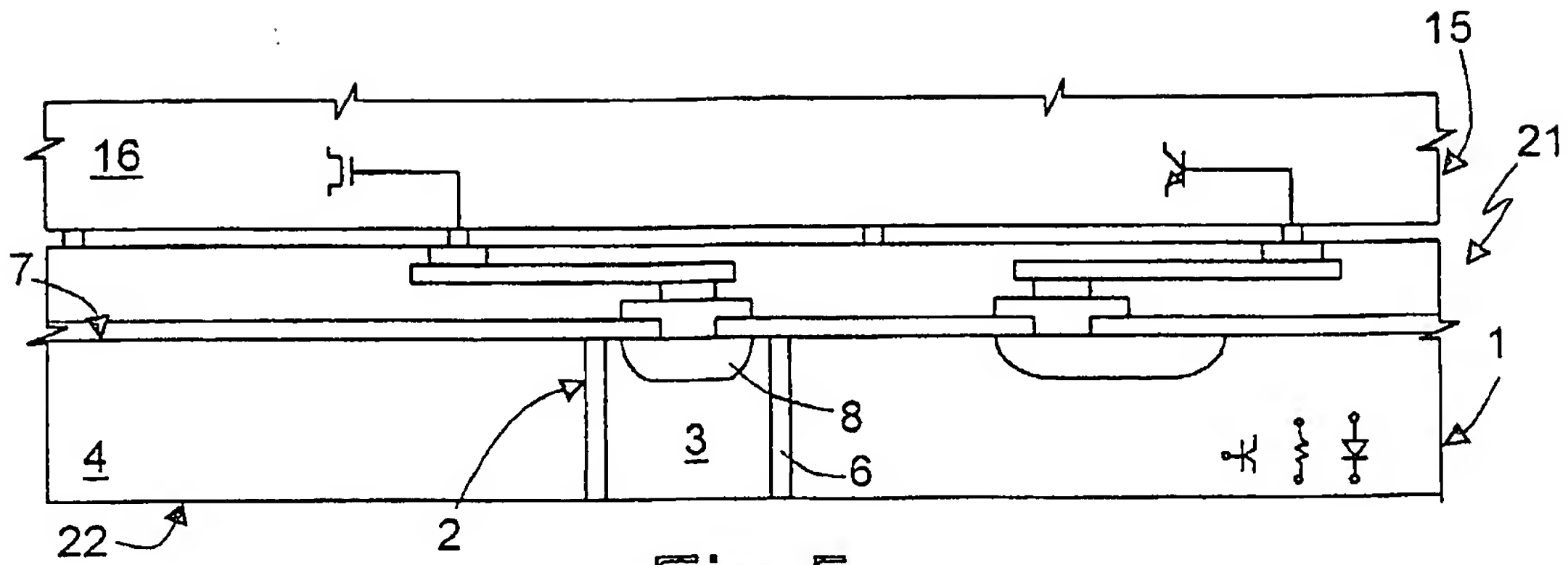


Fig.5

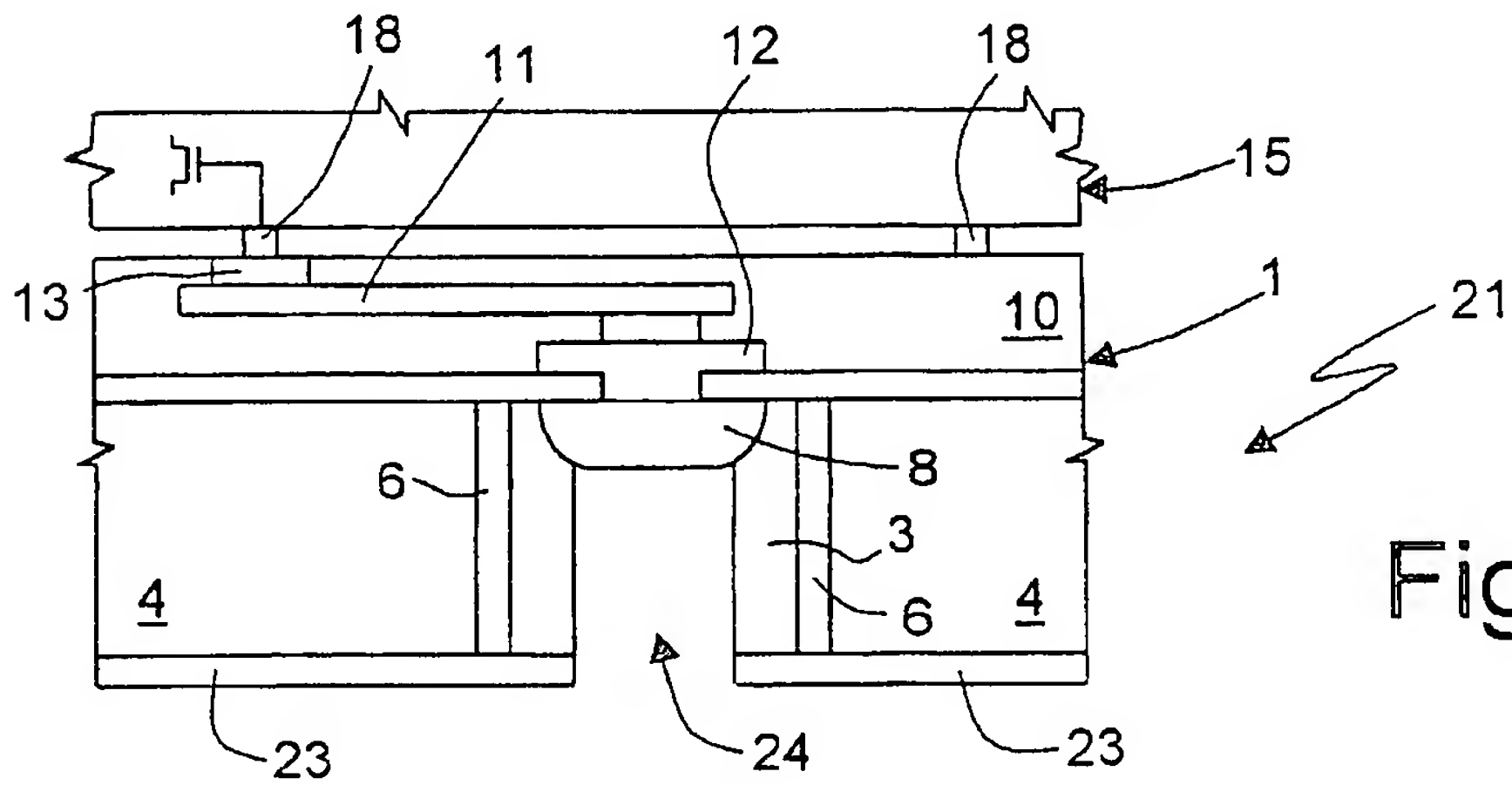


Fig.6

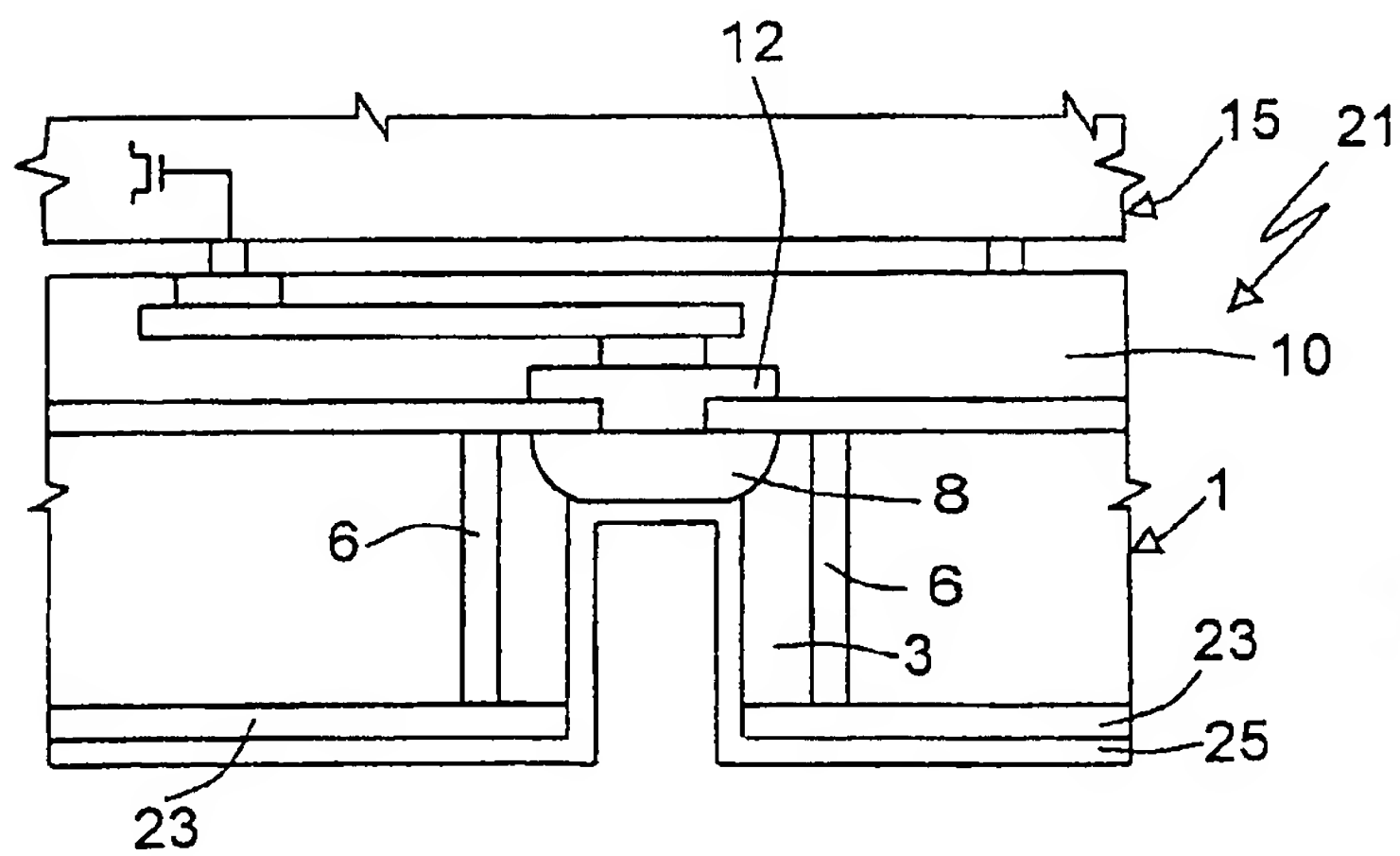


Fig.7

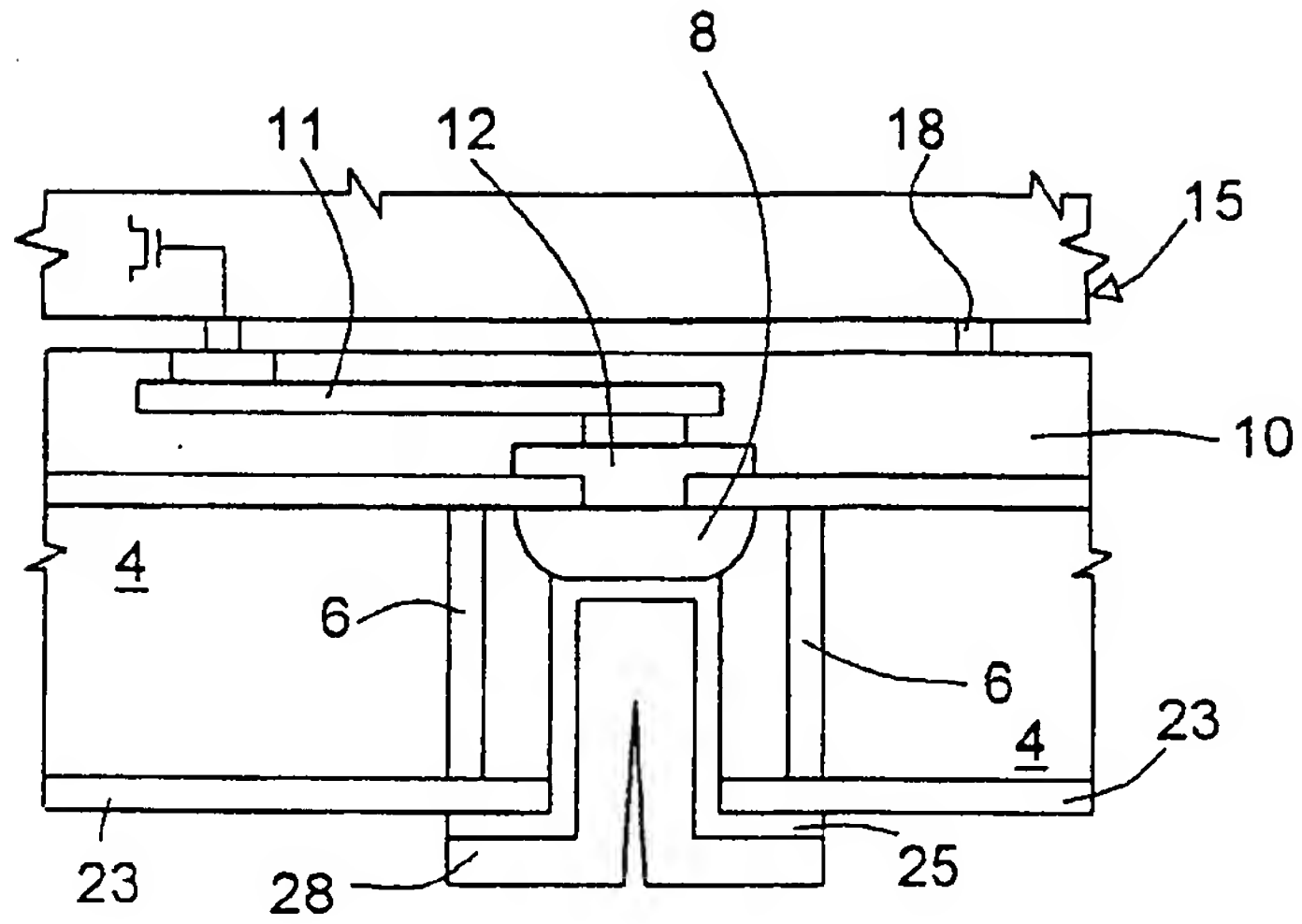


Fig. 8

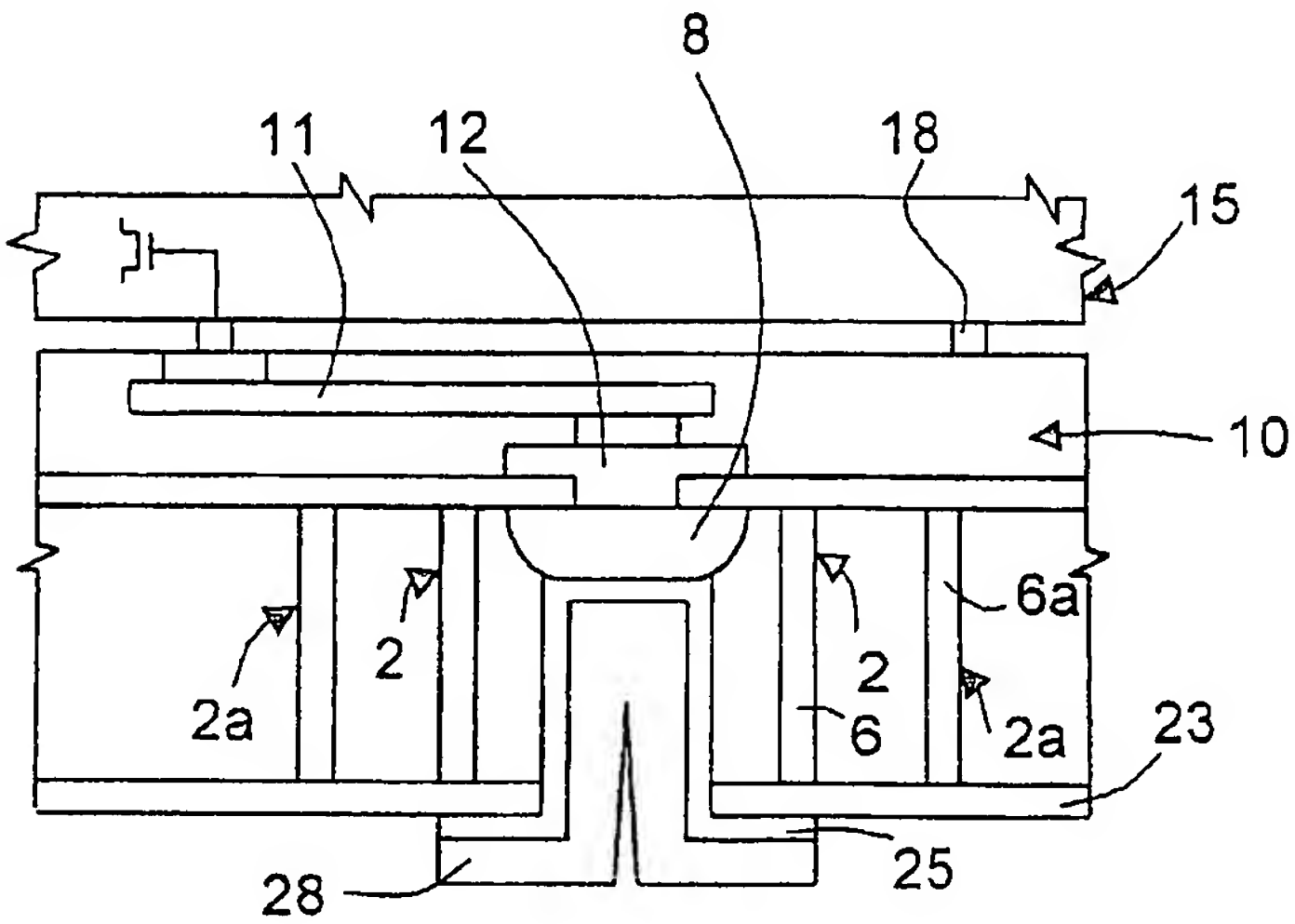


Fig. 9

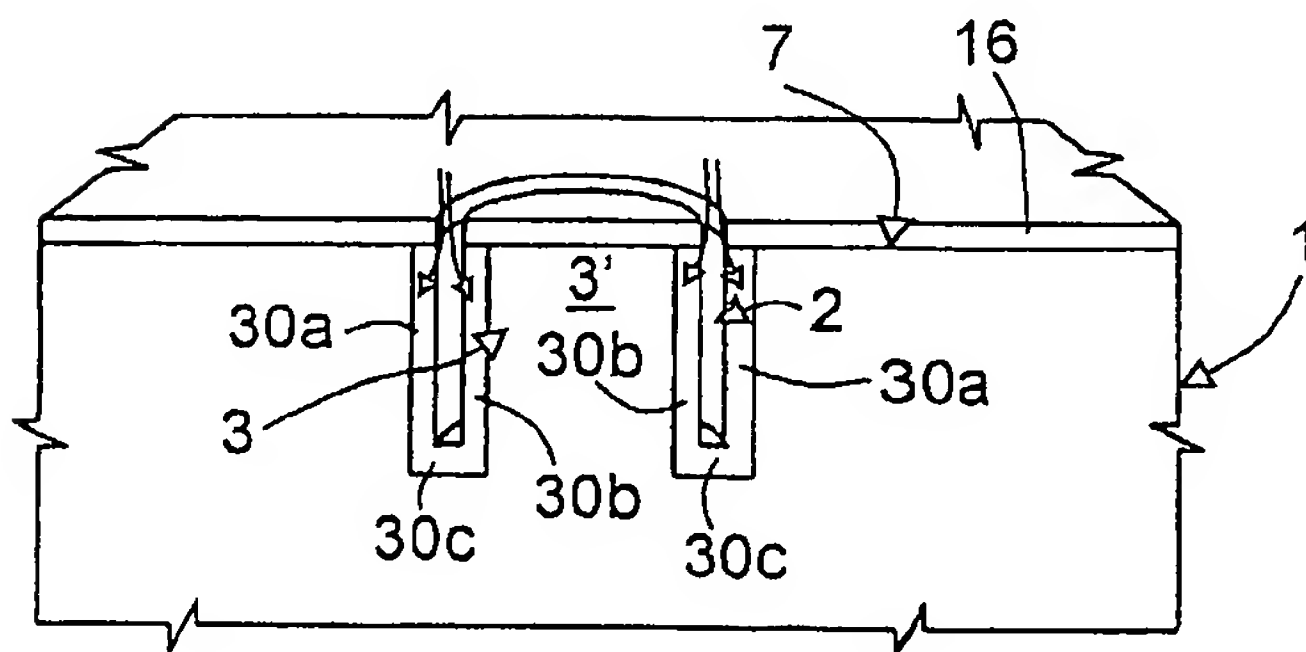


Fig. 10

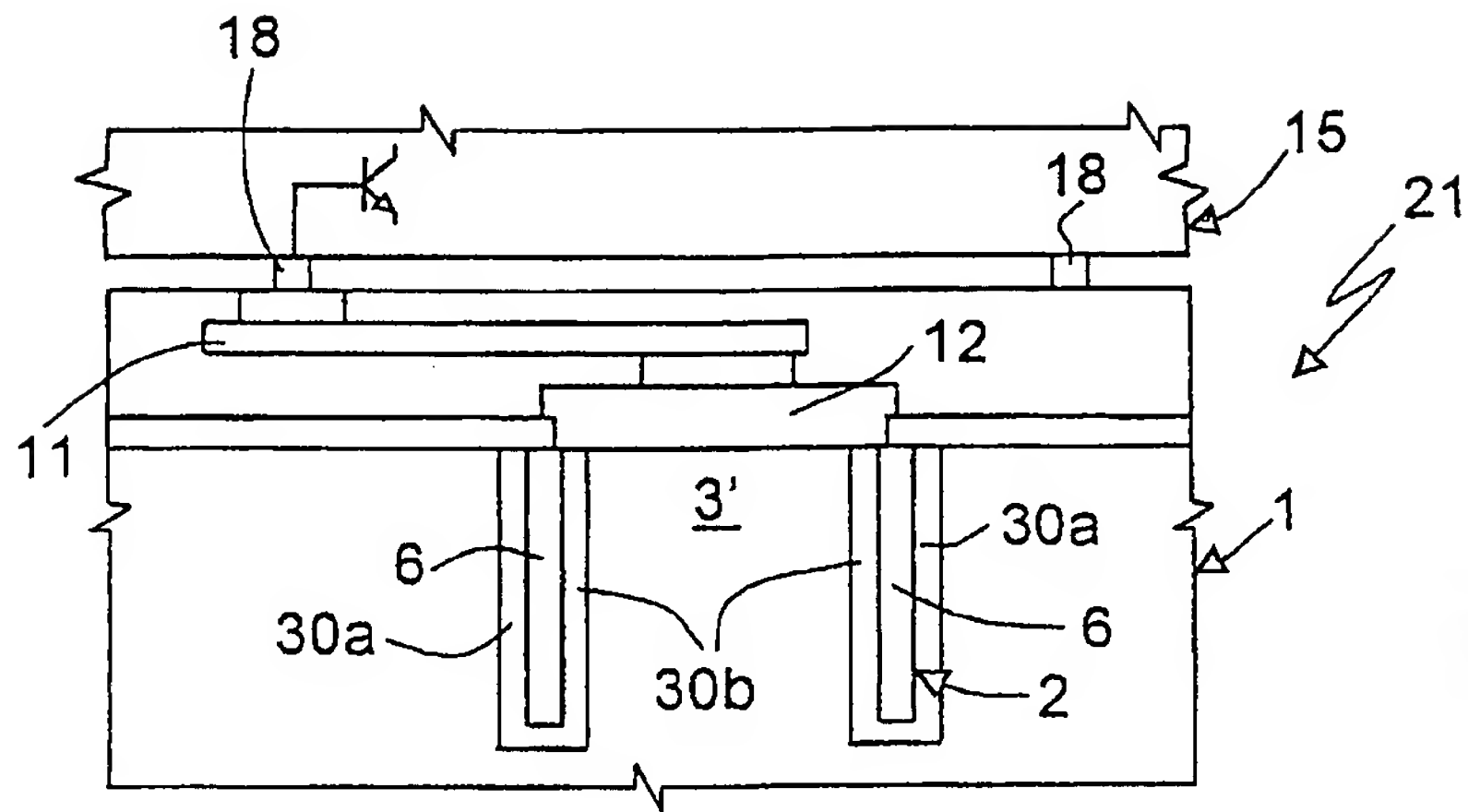


Fig. 11

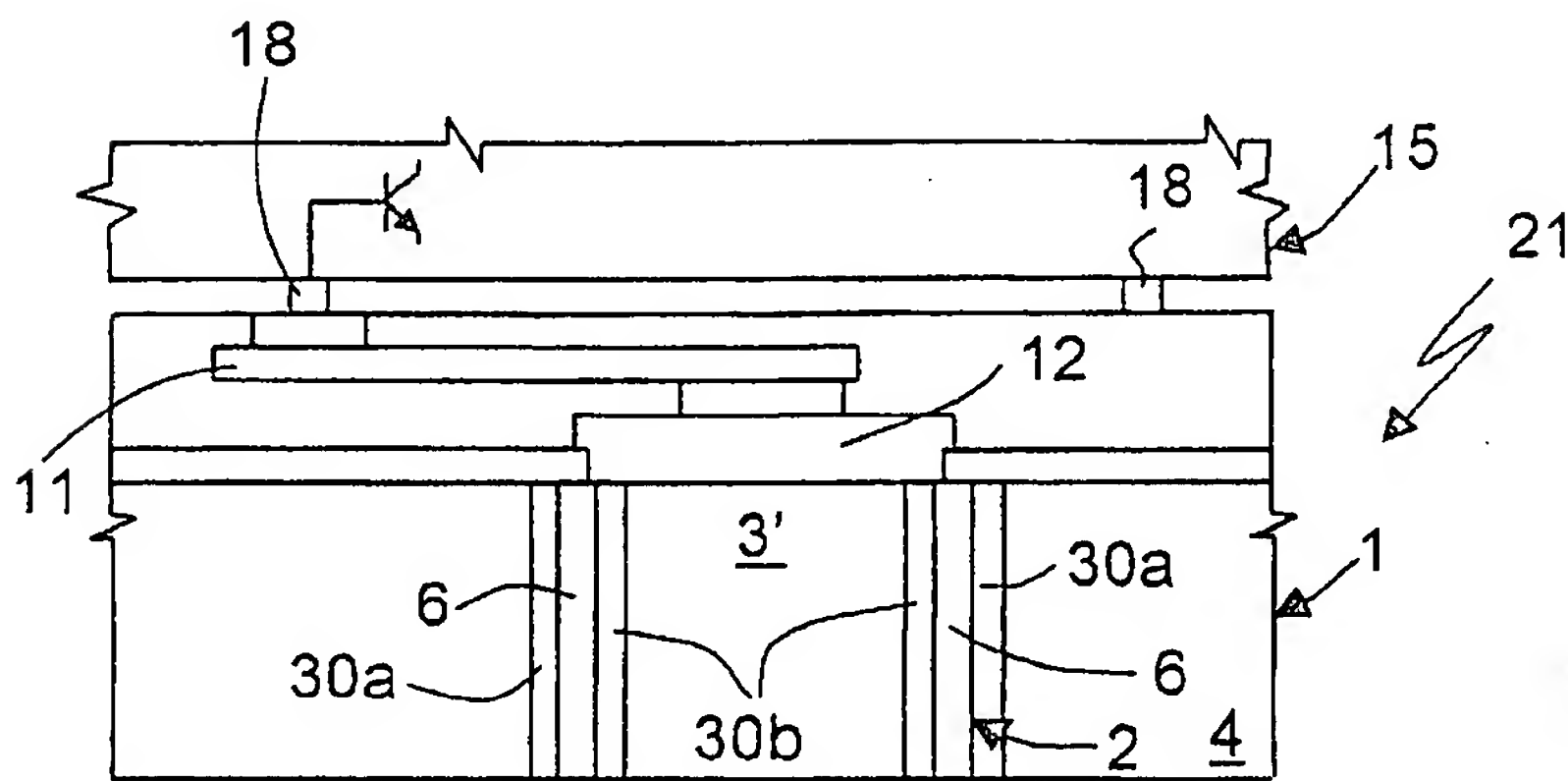


Fig. 12

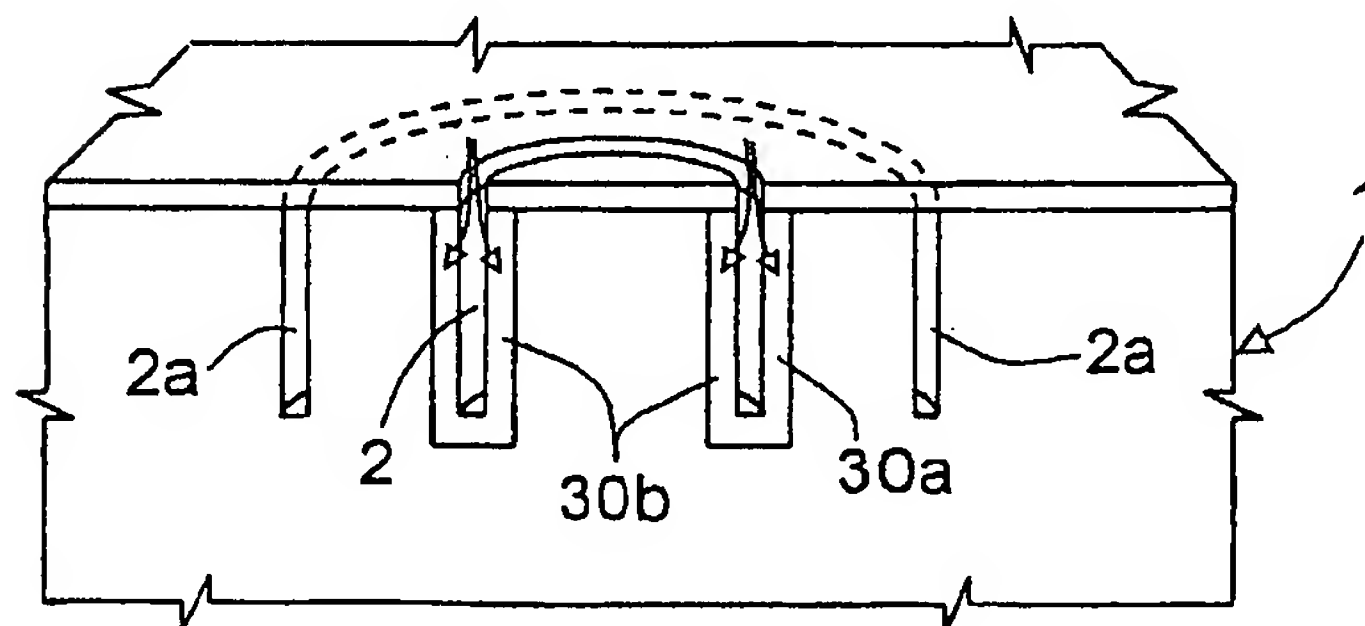


Fig. 14

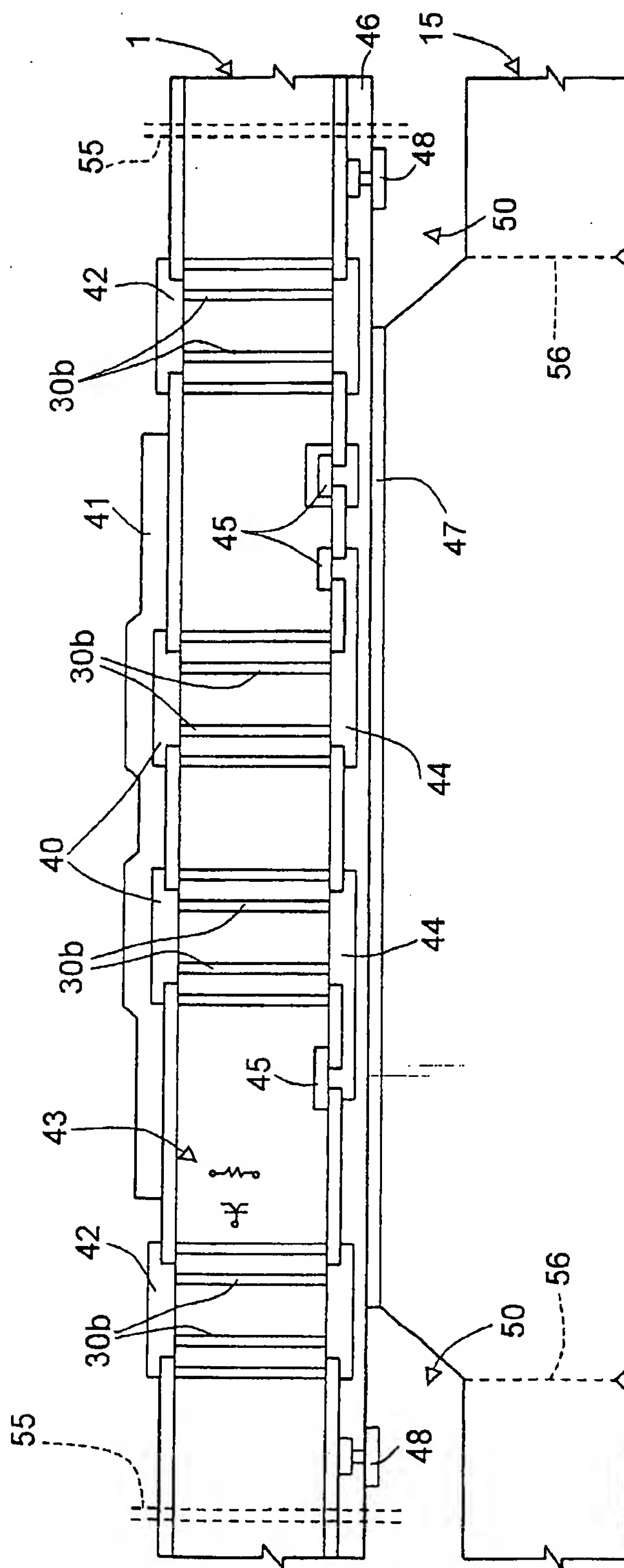


Fig. 13



European Patent  
Office

## EUROPEAN SEARCH REPORT

Application Number  
EP 02 42 5207

DOCUMENTS CONSIDERED TO BE RELEVANT			
Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 95 31006 A (SILICONIX INC) 16 November 1995 (1995-11-16)	1,2,4, 7-10,18, 21-23	H01L21/768
Y		8	
A	* page 9, line 27 - page 14, line 19; figures 2-12 *	5,6,11, 20	
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X	EP 0 926 726 A (ST MICROELECTRONICS SRL) 30 June 1999 (1999-06-30)	1,2,4,7, 9,18, 21-23	
Y	* column 3, line 38 - column 4, line 32 * * column 5, line 34 - column 6, line 13; figures 8,9,16-18 *	5,20	
A		8,10	
	---		
X	DE 198 16 245 A (FRAUNHOFER GES FORSCHUNG) 21 October 1999 (1999-10-21)	1,2,4,9	
A	* the whole document *	12,13, 18,22-24	
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The present search report has been drawn up for all claims			
Place of search THE HAGUE		Date of completion of the search 19 November 2002	Examiner Micke, K
CATEGORY OF CITED DOCUMENTS X: particularly relevant if taken alone Y: particularly relevant if combined with another document of the same category A: technological background O: non-written disclosure P: intermediate document T: theory or principle underlying the invention E: earlier patent document, but published on, or after the filing date D: document cited in the application L: document cited for other reasons &: member of the same patent family, corresponding document			

EPO FORM 1503 03.02 (P04C01)



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 02 42 5207

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The present search report has been drawn up for all claims			TECHNICAL FIELDS SEARCHED (Int.Cl.7)
Place of search THE HAGUE		Date of completion of the search 19 November 2002	Examiner Micke, K
<p>CATEGORY OF CITED DOCUMENTS</p> <p>X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document</p> <p>T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons &amp; : member of the same patent family, corresponding document</p>			

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Application Number

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### CLAIMS INCURRING FEES

The present European patent application comprised at the time of filing more than ten claims.

- ☐ Only part of the claims have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims and for those claims for which claims fees have been paid, namely claim(s):
- ☐ No claims fees have been paid within the prescribed time limit. The present European search report has been drawn up for the first ten claims.

### LACK OF UNITY OF INVENTION

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

see sheet B

- ☒ All further search fees have been paid within the fixed time limit. The present European search report has been drawn up for all claims.
- ☐ As all searchable claims could be searched without effort justifying an additional fee, the Search Division did not invite payment of any additional fee.
- ☐ Only part of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the inventions in respect of which search fees have been paid, namely claims:
- ☐ None of the further search fees have been paid within the fixed time limit. The present European search report has been drawn up for those parts of the European patent application which relate to the invention first mentioned in the claims, namely claims:



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LACK OF UNITY OF INVENTION  
SHEET B

Application Number  
EP 02 42 5207

The Search Division considers that the present European patent application does not comply with the requirements of unity of invention and relates to several inventions or groups of inventions, namely:

1. Claims: 1-13,18-24

Forming a region of higher conductivity inside the region surrounded by the dielectric material,

by forming a contact region of metal material.

2. Claims: 14-17,25,26

Forming a region of higher conductivity inside the region surrounded by the dielectric material,

by forming a contact region having a higher doping level.

**ANNEX TO THE EUROPEAN SEARCH REPORT  
ON EUROPEAN PATENT APPLICATION NO.**

EP 02 42 5207

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on  
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82